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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,105	09/12/2000	David L Losee	81001RLO	6756
1333	7590	05/04/2005	EXAMINER	
PATENT LEGAL STAFF EASTMAN KODAK COMPANY 343 STATE STREET ROCHESTER, NY 14650-2201			HANNETT, JAMES M	
			ART UNIT	PAPER NUMBER
			2612	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/660,105

Applicant(s)

LOSEE ET AL.

Examiner

James M. Hannett

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 1/31/2005 have been fully considered but they are not persuasive. The applicant argues that the prior art does not teach the method wherein the image sensor can be a interline CCD. The applicant further argues that the prior art does not teach that the holes are accumulated substantially at a surface of the image sensor.

The examiner disagrees with the applicant and asserts that the prior art does teach the limitations in question. Burkey et al teaches in the abstract that by placing voltages simultaneously at both electrodes, holes are accumulated at a surface of a substrate in the CCD. Furthermore, Burkey et al teaches on Column 2, Lines 44-47 that the invention can be applied to interline transfer CCD image sensors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1: Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,115,458 Burkey et al in view of USPN 4,468,684 Esser et al.

2: As for Claim 1, Burkey et al teaches on Column 34, Lines 58-68 and depicts in Figure 1 a method for reducing dark current within an image sensor comprising the steps of: Providing the image sensor with a matrix of pixels arranged in a plurality of rows and columns with a vertical shift register (12) allocated for each of the columns and at least one horizontal

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shift register (H) operatively coupled to the vertical shift registers, wherein each of the columns of pixels are formed with the vertical shift registers having a plurality of phases (1 and 2) allocated for each of the pixels and a plurality of gate electrodes of the vertical shift register for each of the pixels, and clocking means for causing the transfer of charge from the pixels to the vertical shift registers and through the horizontal shift register; Burkey et al teaches in Figure 5 and on Column 51-65 and on Column 5, Lines 54-68 applying, at a first time period (Line 6), a first set of voltages to the phases of the gate electrodes of the vertical shift registers sufficient to accumulate holes in the vertical shift register, beneath each gate electrode; Burkey et al teaches on Column 6, Lines 1-11 applying, at a second time period (Line 7), a second voltage to a first set of the gate electrodes while simultaneously applying a more positive voltage to a second set of gate electrodes; Burkey et al teaches on Column 5, Lines 21-23 and Column 6, Lines 1-3 and Column 3, Lines 58-66 applying, at a third time period (stage-to-stage transfer mode), a third voltage to the second set of gate electrodes while simultaneously applying a more positive voltage to the first set of gate electrodes. Burkey et al teaches that a 2-phase shift register is used to transfer charge along the CCD. Burkey et al teaches that the charges on the 1st and 2nd phase lines are changed to allow the charge to transfer from one stage to another. The stage-to-stage transfer is performed after line 7 in Figure 5. During the stage-to-stage transfer, the voltage on (Gate 1) is raised as the gate voltage on Gate 2 is lowered. This allows the charge to transfer to the next pixel location. The polarities are again reversed so the charge is stored under (Gate 1) as depicted in (Line) 1 of Figure 5. Burkey et al teaches on Column 5, Lines 21-24 that (Line 1) depicts the charge configuration at the end of a (stage-to-stage transfer). Burkey et al teaches in the abstract that by placing voltages simultaneously at both electrodes, holes are accumulated at

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a surface of a substrate in the CCD. Furthermore, Burkey et al teaches on Column 2, Lines 44-47 that the invention can be applied to interline transfer CCD image sensors. Burkey et al teaches on Column 5, Lines 54-60 returning the first and second sets of gate electrode voltages to their levels at the first time period.

However, Burkey et al does not specify if the second voltage is of sufficient potential so holes that were accumulated beneath the second set of gate electrodes during the first time are collected and stored beneath the first set of gate electrodes during the second time period; Furthermore, Burkey et al does not specify that the previously accumulated holes beneath the first set of gate electrodes are transferred beneath the second set of gate electrodes.

Esser et al teaches on Column 9, Lines 21-68 and Column 10, lines 1-2 that it is advantageous when operating a CCD shift register to apply the appropriate voltages to the electrodes to allow for the parallel-series transport of holes and electrons. Esser et al teaches that this method is advantageous because during the transport of electrons the electrons can be prevented from flowing back and therefore improve image quality and prevent blooming.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the appropriate voltages as taught by Esser et al to the electrodes of Burkey et al in order to allow for the parallel-series transport of holes and electrons and therefore improve image quality and prevent blooming.

3: In regards to Claim 2, Burkey et al further teaches on Column 5, Lines 31-54 further including the step of applying voltages (performing steps 2-5) to the first and second sets of gate electrodes between the third applying step (step-to-step transfer) and the returning step (Line 6) to cause excess charge to be returned under the preceding gate electrode.

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4: As for Claim 3, Burkey et al further teaches on Column 3, Lines 51-54 the vertical shift registers are two-phase devices. Burkey et al teaches the use of transferring the charge using a 2-phase driven shift register. However, Burkey et al does not teach that the voltage magnitudes of the two clock signals are equal.

Official notice is taken that it was well known in the art at the time the invention was made that when operating a 2-phase vertical shift register in a CCD to drive the two phases with voltage magnitudes that were equal to each other in order to better transfer charge along the CCD.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the magnitudes of the 2-phase clock signals equal to each other in order to better transfer charge along the CCD.

5: In regards to Claim 4, Burkey et al further teaches on Column 4, Lines 3-10 wherein the step of applying the first voltage to the phases of the vertical shift registers occurs during a readout period of the horizontal shift register. Burkey et al teaches that the horizontal shift register is actuated by the same voltage signal lines that transfer charge in the vertical shift register.

6: As for Claim 5, Burkey et al further teaches on Column 2, Lines 44-47 wherein the image sensor is an interline transfer type image sensor.

Allowable Subject Matter

7: Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Hannett whose telephone number is 571-272-7309. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
April 22, 2005


WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600